CLAIMS

What is claimed is:

1. A magnetic memory cell comprising:

a magnetic tunneling junction including a first ferromagnetic layer, a second ferromagnetic layer and an insulating layer between the first ferromagnetic layer and the second ferromagnetic layer; and

a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell.

2. The magnetic memory cell of claim 1 wherein the transistor is a MOSFET or another type of transistor.

3. The magnetic memory cell of claim 1 wherein a second end of the magnetic tunneling junction and the source of the transistor are coupled to ground.

4. The magnetic memory cell of claim 1 wherein the transistor is operated in a saturation region during reading.

5. A magnetic memory comprising:

a plurality of memory cells arranged in an array including a plurality of rows and a plurality of columns, each of the plurality of memory cells including a magnetic tunneling junction and a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end of the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell;

a plurality of row lines coupled to the plurality of rows, the plurality of row lines coupled to gate of the transistor in each of the plurality of memory cells in the plurality of rows;

a row selector coupled to the plurality of row lines for selecting between the plurality of row lines and providing a current to a selected row of the plurality of rows.

6. The magnetic memory of claim 5 further comprising:

a first plurality of column lines coupled to the plurality of columns, the plurality of columns lines coupled to source of the transistor in each of the plurality of memory cells in the plurality of columns;

a second plurality of column lines coupled to the plurality of columns, the second plurality of column lines coupled to the drain of the transistor in each of the plurality of memory cells in the plurality of columns, each of the first plurality of columns lines coupled to a particular column, a corresponding column line of the second plurality of column lines coupled to the particular column line, each of the first plurality of column lines and the corresponding column line of the second plurality of column lines forming a pair of column lines;

a column selector coupled to the first plurality of column lines and the second plurality of column lines for selecting between the first plurality of column lines and the second plurality of column lines to select a pair of column lines.

7. The magnetic memory of claim 5 further comprising:

a plurality of digit lines for providing a current for writing to a portion of the plurality of memory cells.

8. The magnetic memory of claim 6 further comprising a load coupled to the plurality of column lines.

9. The magnetic memory of claim 5 wherein the transistor is operated in a saturation region during reading.

10. A method for utilizing a magnetic memory comprising the steps of:

(a) during writing, writing to a first portion of a plurality of memory cells, the plurality of memory cells arranged in an array including a plurality of rows and a plurality of columns, each of the plurality of memory cells including a magnetic tunneling junction and a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end of the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell;

(b) during reading, reading from a second portion of the plurality of memory cells.

11. The method of claim 10 wherein the reading step (b) further includes the steps of:

(b1) selecting the second portion of the plurality of memory cells using a plurality of row lines coupled to the plurality of rows, the plurality of row lines coupled to gate of the transistor in each of the plurality of memory cells in the plurality or rows, the second portion of the plurality of memory cells being selected by providing a constant current to a portion of the plurality of row lines coupled to the second portion of the plurality of memory cells.

12. The method of claim 10 wherein the reading step (b) further includes the steps of:

(b1) selecting the second portion of the plurality of memory cells using a plurality of column lines coupled to the plurality of columns, the plurality of column lines providing a load to the second portion of the plurality of memory cells.

13. The method of claim 10 wherein the reading step (b) further includes the step of:

(b1) reading data from the output coupled with the drain of the transistor of each memory cell of the second portion of the plurality of memory cells.

14. The method of claim 10 wherein the writing step (a) further includes the steps of:

(a1) selecting the first portion of the plurality of memory cells using a portion of a plurality of digit lines, the portion of the plurality of digit lines providing a write current.

15. The method of claim 10 wherein the writing step (a) further includes the step of:

(a1) selecting the first portion of the plurality of memory cells using a portion of the plurality of row lines coupled to the plurality of rows, the plurality of row lines providing a write current during writing to the first portion of the plurality of memory cells.

16. The method of claim 10 wherein the reading step (b) further includes the step of:

(b1) operating the transistor in a saturation region during reading.